REMARKS

This application has been amended so as to place it in condition for allowance at the time of the next Official Action.

The Official Action rejects claims 3 and 12 under 35 USC 112, second paragraph, as being indefinite. The Official Action also objects to claim 6. Applicant has amended each of claims 3, 6, and 12 to eliminate the identified bases for rejection and objection in accordance with the helpful recommendations provided by the Official Action. Reconsideration and withdrawal of both the rejection and the objection are therefore respectfully requested.

The Official Action rejects claims 3, 4, 12, 13, 20, and 23 under 35 USC 102(e) as anticipated by RUB. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

Of the rejected claims, claims 3 and 12 are independent. Each of claims 3 and 12 is directed to the serial-to-parallel function of the present invention, with claim 3 directed to a serial communication device and claim 12 to a method of carrying out serial communication. By either device or method, serial data with an error correction code incorporated therein is converted ultimately into parallel data. Also in each claim, the conversion is not achieved in a single step.

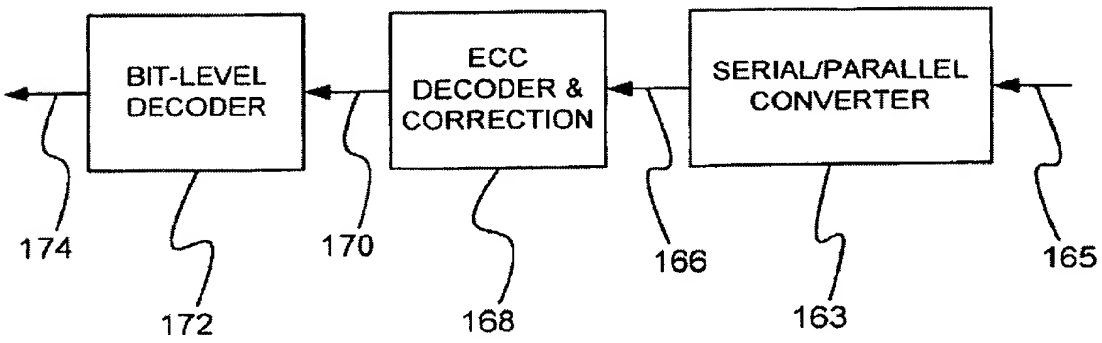
Instead, the serial data with the error code incorporated therein is first converted into parallel arrangement

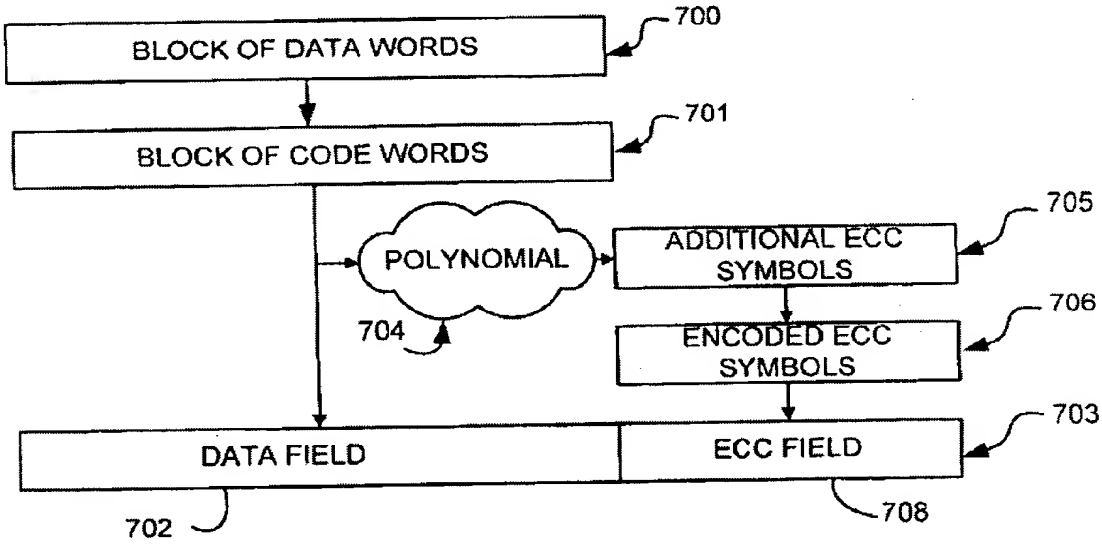
of data and an error correcting code which, in a subsequent step, is converted into a wider parallel bus. One way to consider the present invention is to envision it as starting with serial data with the error codes incorporated therein which is first converted into byte-wide parallel data with error codes. The bytes with the included error codes are then demultiplexed onto a parallel bus of data. While the first parallel bus described above is only a single byte wide, the final parallel bus is some multiple number of bytes wide. Accordingly, the data transitions from serial with error correcting code into a relatively narrow parallel bus with error correcting code and then into a wide bus.

The RUB reference fails to explicitly disclose multiplexing parallel buses and the necessity of carrying out conversion between parallel data and serial data.

In the present device, the conversion between parallel data and serial data is carried out for the purpose of cost reduction in communication between redundant processors and reduction of defects in the fabrication of a serial communication device.

The Official Action interprets the recited elements of the rejected claims as reading on the parallel-to-serial portion of the RUB device illustrated, for example, in Figure 2. A portion of Figure 2 is reproduced below.





In the RUB device, serial data with error correcting code bytes incorporated therein is represented as 165. The serial data then enters the serial-parallel converter 163 and emerges as the ECC code word 166. The ECC code word 166 corresponds to element 703 as illustrated in Figure 7 of RUB, also reproduced above. The ECC code word is then passed to the ECC decoder and correction module 168 in RUB. It emerges from there as the data code word 170. The code word corresponds to element 701 of Figure 7. At this point, the data codes have been stripped off

and analyzed based on the interpretation of such codes, the data is passed through, corrected, or flagged as erroneous.

The data code words 170 are then passed to the bit-level decoder 172, from which they emerge as data words 174. The data words correspond to element 700 of Figure 7.

The serial-parallel converter element of claim 3 and corresponding converting step of claim 12 can reasonably be read on the structure and function of the serial-parallel converter 163 of RUB. If this is the case, however, the output of the serial-parallel converter 163 of RUB must be *n* bit wide parallel data segments and error correcting code included in both claims.

Claim 3 next recites an error detector, and method claim 12 recites steps of checking the error correcting code and checking for an error. This structure and function can reasonably be read on the error decoder and correction element 168 of RUB.

The final step of independent claim 12, however, entails the demultiplexing of the *n* bit wide parallel data segments into *m* bit wide parallel data on the parallel bus, with $m > n$. The recited component of the device of claim 3 similarly receives as an input parallel data which it demultiplexes onto a separate parallel bus. The conversion of an encoded data word into a non-encoded data word as performed by the bit-level decoder 172 of RUB cannot reasonably be interpreted as a demultiplexing function, as is required by both of independent

claims 3 and 12. Moreover, the specific recitation of the *m* bit wide parallel bus being of greater width than the *n* bit wide parallel bus is not indicated anywhere in the RUB reference. Neither the text of the RUB reference nor the drawing figures thereof provide any indication that the bus 174 is wider than the bus 170, or that the bus 174 reflects a demultiplexed version of the bus 170.

For at least these reasons, applicants respectfully suggest that the applied reference fails to disclose the features of independent claims 3 and 12, and, by extension, any of the claims 4, 13, 20, and 23, which depend therefrom.

The Official Action rejects claims 1, 10, 19, and 22 under 35 USC 103(a) as being unpatentable over GOTZE et al. in view of CARLTON et al. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

Of the rejected claims, claims 1 and 10 are independent. Each of the independent claims contemplates an invention which, overall, receives a parallel bus and generates serial data with error codes incorporated therein. Claim 1 recites the invention as a device, and claim 10 as a method.

As with the independent claims considered in the previous anticipation rejection over RUB, the invention of claims 1 and 10 embodies an intermediate step or component, in which the relatively wide input bus is first converted into a narrower parallel bus via a multiplexer, the narrower parallel bus is

accompanied by an error correcting code. The narrow bus with the error correcting code is then, in a second step, converted to an entirely serial arrangement of data with the error correcting code incorporated therein.

The Official Action identifies as the structure of the GOTZE et al. device interpreted as meeting the recited features as that illustrated in Figure 2 of the reference. Figures 1 and 2 of the GOTZE et al. are reproduced immediately below:

FIG.1

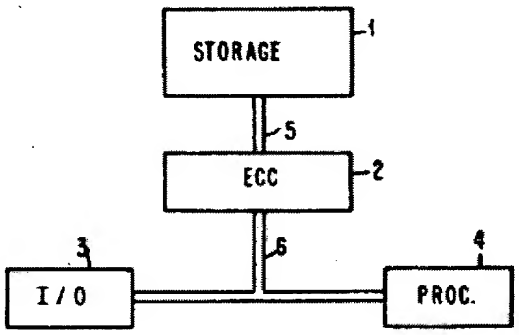
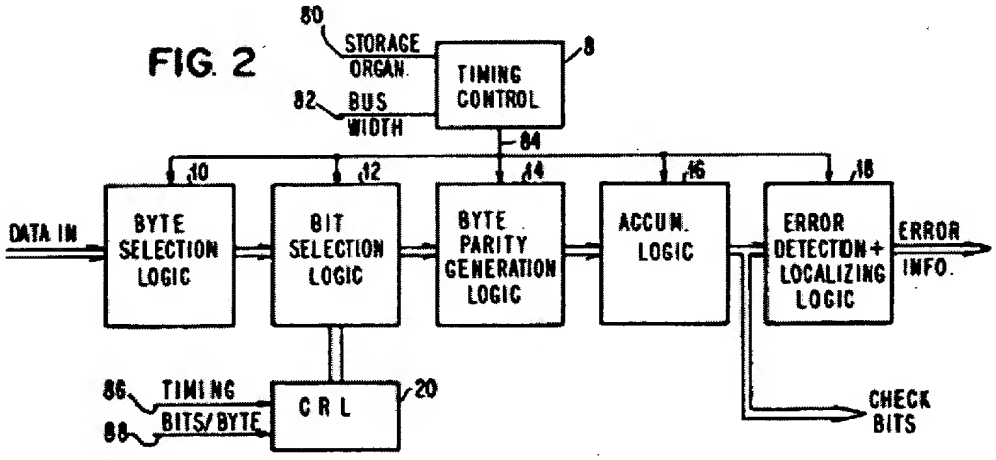


FIG. 2



The Official Action identifies the byte selection logic 10 illustrated in Figure 2 of the reference as the parallel bus interface circuit that receives *m* bit wide data from the parallel bus and multiplexes the same into sequentially generated *n* bit wide parallel segments. The check bit producer of claim 1 and corresponding applying step of method claim 10 require the input of an *n* bit wide parallel data segment and the output of a parallel arrangement of the same *n* bit wide parallel data segment and a generated error correcting code. Accordingly, this step requires parallel data in and corresponding parallel data out, with the output accompanied by the appropriate error correcting code.

The Official Action relies on language in column 3, lines 19-20 that describe the check bits as being generated byte-wise. What the reference fails to disclose, as does all other known prior art, is the input of a *n* bit wide parallel data segment, which itself is produced as a subset of an overall *m* bit wide data bus, and the output of the same *n* bit wide parallel data segment with a generated error correcting code placed in parallel therewith.

It is particularly useful to consider what is received into and generated by each of the successive elements illustrated in Figure 2 of GOTZE et al. The byte selection logic 10 might be construed as receiving as an input a full width bus and generating therefrom one selected byte out of a multi-byte word.

That selected byte, with no error correcting code attached, is then forwarded to the bit selection logic 12. As described in column 3, beginning on line 49, the bit selection logic 12 selects for each data byte those data bits that are to be used for generating the check bit. Accordingly, the output of the bit selection logic 12 is a set of bits that represents a subset of the bits that make up the selected byte, again with no error correcting code attached.

The byte parity bit is then generated by the byte parity generation logic 14. Therefore, the output of element 14 is no data that can, in itself, be tied uniquely to the data and received by the byte selection logic. At this point in the sequence, while an error correcting code may exist at the output of element 14, the data no longer exists. The individual byte parities are summed in a defined manner in the accumulation logic 16, as described beginning on line 55 of the same column of the reference. Accordingly, there is at no point in the sequence of steps or structure presented by GOTZE et al. a point where there exists an arrangement of parallel data that represents a subset of a larger parallel data arrangement, with the subset parallel data having an attached error correcting code.

This derives principally from the fact that the entire structure illustrated in Figure 2 of GOTZE et al. is not an arrangement through which the data identified as "DATA IN" at the left of Figure 2 passes. Instead, the actual data takes a

parallel, direct route past all of the structure illustrated in Figure 2. That same data is split off to the byte selection logic 10 of Figure 2 in order to generate the necessary check bits and/or error information. However, the data itself never exits the structure of Figure 2.

Accordingly, as is the case with the RUB reference, there exists no arrangement of a parallel bus being multiplexed into a narrower parallel bus with associated error correction code, which is in turn converted into serial form.

The Official Action acknowledges that the GOTZE et al. reference does not explicitly disclose a parallel-serial converter. It is this feature for which the secondary CARLTON et al. reference is offered. However, the CARLTON et al. reference nevertheless fails to overcome the shortcomings of the primary reference, as the secondary reference also fails to provide any teaching or suggestion of an arrangement in which a wide parallel bus is multiplexed into a narrower parallel bus with associated error correction code.

For all of the reasons presented above, applicants respectfully suggests that the present rejection of claims 1, 10, 19, and 22 over GOTZE et al. in view of CARLTON et al. cannot reasonably be maintained.

The Official Action rejects claims 5, 14, 15, 17, 18, 24, and 26 under 35 USC 103(a) as being unpatentable over RUB in view of GOTZE et al. Each of the references applied in this

rejection has been considered in detail in one of the preceding rejections. As is evident from such analysis, neither such references teaches the wide parallel/narrow parallel with correction code/serial arrangement, or its reverse, which underlies each of the independent claims under consideration, and is therefore implicitly recited in each of the claims that depends therefrom. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

The Official Action explicitly states that claims 6, 8, 9, 21 and 25 are allowed. In light of the analysis provided above, applicant respectfully suggests that both the identified allowed claims as well as all other claims remaining in the application are in condition for immediate allowance, and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires further clarification of any of the above points, the Examiner may contact the undersigned attorney so that this application may continue to be expeditiously advanced.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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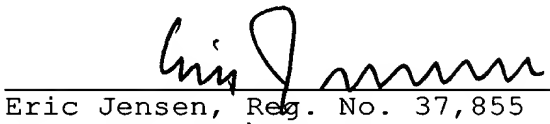

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